# PureB silicon photodiode detectors for DUV/VUV/EUV light and low-energy electrons

#### Lis K. Nanver

Delft Institute of Microsystems and Nanoelectronics – DIMES Delft University of Technology



30<sup>th</sup> August, 2011





## Acknowledgements

 PhD students: Lei Shi, Gianpaolo Lorito, Agata Šakič, Francesco Sarubbi, Negin Golshani, Vahid Mohammadi, Lin Qi
Postdocs: Caroline Mok, Jaber Derakhshahdeh
Process technologists: Tom Scholtes, Wiebe de Boer, Silvana Milosalvjevic, Wim Wien, Carel Heerkens

ASML Lithography: Stoyan Nihtianov, Koen Kivits, René de Bruin FEI Company: Gerard van Veen, Kees Kooijmanns, Patrick Vogelsang PTB Berlin: Frank Scholze, Christian Lauber, Andreas Gottwald, Ulrich Kroth



# Outline

- Introduction
- Pure boron CVD technology
- Doping from pure boron layers
- Electrical properties of PureB p+n diodes
- Application as photodetectors for low-penetration-depth radiation and charged particles :
  - VUV, DUV, EUV
  - low-energy electrons
- Conclusions



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# Pure boron CVD technology



Pure boron deposition from  $B_2H_6$  gas in an AMSI Epsilon One Si/SiGe epitaxial CVD reactor



700°C deposition Not visible on the

HRTEM: a few nm B-doping of the c-Si below the B<sub>x</sub>Si<sub>v</sub>  $\alpha$ -B ~ 4 nm

 $B_x Si_v \sim 1 \text{ nm}$ 

Crystalline Si substrate





# **Constant boron deposition rate**



 $B_2H_6$  flow rate: 490 sccm



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# **Other boron deposition properties**

#### Under the right conditions:

• high selectivity to native-oxide-free Si surfaces

 $\alpha$ -Si

Uniform coverage

• uniform depositions for temperatures: 500 °C – 700 °C

**B-layer** 

• isotropic deposition on Si

SiO,

50 nm



Isotropic deposition



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# **Doping from pure boron layers**





# **Doping from pure boron layers**



5 s exposure: ~ 1 monolayer =  $6.78 \times 10^{14}$  cm<sup>-2</sup>

10 min exposure: ~  $10^{17}$  cm<sup>-2</sup>



# **B-layer removal**



After B-layer removal: ~  $10^{14}$  cm<sup>-2</sup> boron concentration left This exceeds the solid solubility  $\Rightarrow$  some B<sub>x</sub>Si<sub>y</sub>



## Sheet resistance measurements



B-layer resistivity very high: 10<sup>4</sup> ohm-cm (semi-metal) Doping of Si dominates sheet resistance **TUDelft** 12 **Post-processing for reduction of series resistance** 

in-situ thermal annealing and/or selective epitaxial Si/SiGe growth:



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# **Enhanced diffusion effects**

No real evidence of transient or boron enhanced diffusion has been found



Epitaxially-grown boron marker before and after PureB-deposition:

difference within experimental uncertainty



# **Electrical test structures**



(1) p<sup>+</sup>n diodes n-doping ~  $10^{17}$  cm<sup>-3</sup>



(2) pnp bipolar transistorsemitter = B-layer

B-layer deposited in contact window, metallized immediately with Al/Si(1%)

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# p<sup>+</sup>n forward diode characteristics



Same behaviour at both temperatures:

- ideal characteristics
- saturation current decreases with deposition time
- series resistance first decreases and then increases



# p<sup>+</sup>n reverse diode characteristics



High electric field at perimeter lowers breakdown voltage

Use guard ring, but not seen for low substrate doping

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# pnp transistor characteristics



Base current level decreases with deposition time

1 min attractive:

- current gain comparable to conventional implanted-emitter pnp
- series resistance low

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# pnp transistor characteristics



The B-layer suppresses the injection of electrons from the substrate  $\Rightarrow$  B-layer thickness determines the current gain Sarubbi, IEEE-TED 2010

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# Lithography roadmap down to 10 nm features

# EUV: supports 22 nm and 16 nm nodes with a single projection system



# **Challenging DUV/VUV/EUV detection**



# **Challenging DUV/VUV/EUV detection**



Ideal spectral responsivity of Si-based photodetectors



# **Optical performance**

#### EUV optical performance



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Measured spectral responsivity of EUV PureB diodes with a 2.5 min Bdeposition compared with a commercial  $n^+p$  photodiode and the theoretically attainable values for an ideal Si-based photodetector.

# **Optical performance**

DUV/VUV optical performance



Measured responsivity of PureB-diodes in DUV/VUV spectral range compared with other state-of-the-art photodetectors.



# **Performance stability**

#### EUV responsivity degradation



shape of the EUV spot (irradiance in the high power region is 3 W/cm<sup>2</sup> [24]) and the EUV-induced carbon contamination layer.

Ratio of measured EUV spectral responsivity after/before intense EUV irradiation (220 kJ/cm<sup>2</sup>), compared to the calculated ratio of responsivity based on the same diode with/without a 20 nm carbon layer



# **Performance stability**

DUV/VUV responsivity degradation



 $\sim$  4 nm silicon oxide layer was measured on the diode surface



# **Performance stability**

#### DUV/VUV responsivity degradation



#### Oxide-free boron surface



#### **High Stability**



# Robustness

#### H\* cleaning



Filament enhanced H\* cleaning setup



Plasma-generated H\* cleaning setup



Micro-image of the EUV contaminated sample before / after 2 hours' H\* cleaning.



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#### Crucial throughput requirement: 100 wafers per hour

**Mirrors not lenses** 

Energy sensor

EUV source: the most difficult challenge

2 wafer stages

ASML

TIS (transmission imaging sensor)

Spot/slit sensor

**3 types of detectors developed by DIMES** 

# **EUV Product Roadmap**



#### 2006

ADT Resolution = 32 nm NA = 0.25,  $\sigma$  = 0.5 Overlay < 7 nm Throughput 5 WPH @ 5mJ/cm<sup>2</sup> ~8W

#### Main improvements

- 1) New EUV platform :NXE 2) Improved low flare optics
- 3) New high σ illuminator
- 4) New high power LPP source
- 5) Dual stages



#### 2010

#### NXE:3100

Resolution = 27 nm NA = 0.25,  $\sigma$  = 0.8 Overlay < 4.5 nm Throughput 60 WPH @ 10mJ/cm2 >100W

#### Main improvements

1) New high NA 6 mirror lens

- 2) New high efficiency illuminator
- Off-Axis illumination option
- Source power increase
- 5) Reduced footprint



#### 2012

#### NXE:3300B

Resolution = 22 nm NA = 0.32,  $\sigma = 0.2-0.9$ Overlay < 3.5 nm Throughput 125 WPH @ 15mJ/cm2 >350W



#### 2013

#### NXE:3350C

Resolution = 16\* nm NA = 0.32, OAI Overlay < 3 nm Throughput 150 WPH @ 15mJ/cm2 >550W

#### Platform enhancements 1) Source power increase

\* Requires <7nm resist diffusion length



Detector elements: photodiodes

#### Good manufacturability

- IC processing compatibility
- flexibility

temperature sensors

absorber layer stacks

different filter layer stacks

5 different types of alignment marks

two-sided contacting

excruciating electrical, optical and mechanical specifications

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# **Low-Energy Electron Detection**

Challenges: low range in Si



# **Device fabrication**





# **Device fabrication**







# **Relative Electron Signal Gain**



 $G_{R}(E_{beam}) = \frac{I_{ph} / I_{beam}}{(E_{beam} / e_{0})(1 - \eta)} = \frac{G_{PH}}{G_{TH}}$  $G_{R} = 0 \longrightarrow I_{ph} = 0$  $G_{R} = 1 \longrightarrow G_{PH} = G_{TH}$ 

State-of-art commercial detectors:

- vCD: low Voltage high Contrast Detector
- BSE: Backscattered-electron detector





## **FEI electron detectors**

- Special requirements: very low capacitance low resistance many separated detector segments through-wafer holes
- Solutions: low doped, high-quality, 40 µm thick epi-layers special metal grid processing through-wafer deep dry etching



# Example of imaging capability (FEI ASB Magellan SEM)



SEM images of pollen taken with B-layer detectors

Sakic, IEDM 2010





# **Future processes**



# Selective Ge epitaxy on Si

- Unique feature: Large islands possible with sub-300nm transition at 700°C
- Uniform Ge surface compatible with CMOS planar processing



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# **Ge-dots embedded in Si: defect-free**



A  $\mu$ -Raman strain measurement in the silicon above an embedded Ge quantum-dot [2]. Huandra, Nanoletters 2011



# The first PureB application:

high-Q high-linearity varactor circuits made in silicon-on-glass technology





# SOG varactor diodes

# True Two-sided contacting: ideal 1-D behavior eliminate parasitics



Diodes: low leakage, ultrashallow, made at low temperature